What is Claimed is:

[c1] A method for forming a transistor, the method comprising the steps of:

providing a semiconductor wafer having a semiconductor layer overlying a buried insulator having at least two layers;

forming a first recess and a second recess through the semiconductor layer and a first layer of the buried insulator;

forming a body from the semiconductor layer situated between the first recess and the second recess so that a top body surface and a bottom body surface define a body thickness; and

forming a source structure having a source region into the first recess and forming a drain structure having a drain region into the second recess so that a top portion of the source structure and a top portion of the drain structure are within and abut the body thickness.

[c2] The method of claim 1, wherein the step of providing a semiconductor wafer comprises providing a semiconductor wafer having a semiconductor layer overlying a buried insulator having at least two layers so that a first layer of the buried insulator is at least as thick as the semiconductor layer.

[c3] The method of claim 1, wherein the step of providing a semiconductor wafer comprises providing a semiconductor wafer having a semiconductor layer comprising single crystal silicon overlying a buried insulator having at least two layers.

[c4] The method of claim 1, wherein the step of providing a semiconductor wafer comprises providing a semiconductor wafer having a semiconductor layer overlying a buried insulator having three layers so that a second layer is different from a first layer and a third layer.

[c5] The method of claim 4, wherein the step of providing a semiconductor wafer comprises providing a semiconductor wafer having a semiconductor layer overlying a buried insulator having the first layer comprising silicon dioxide, the second layer comprising silicon nitride, and the third layer comprising silicon dioxide.

[c6] The method of claim 1, wherein the step of forming a first recess and a second recess further comprises stopping on a second layer of the buried insulator.

[c7] A method of claim 1, wherein the step of forming a body comprises forming a fin

structure from the semiconductor layer situated between the first recess and the second recess so that a top fin structure surface and a bottom fin structure surface define a fin structure thickness, wherein the step of forming a source structure and a drain structure comprises forming a source structure having a source region into the first recess and forming a drain structure having a drain region into the second recess so that a top portion of the source structure and a top portion of the drain structure are within and abut the fin structure thickness.

[c8] A transistor comprising:

a semiconductor wafer comprising a semiconductor layer overlying a buried insulator having at least two layers;

a first recess and a second recess formed through the semiconductor layer and a first layer of the buried insulator;

a body formed from the semiconductor layer situated between the first recess and the second recess, the body comprising a top body surface and a bottom body surface that define a body thickness;

a source structure formed into the first recess, the source structure comprising a source region; and

a drain structure formed into the second recess, the drain structure comprising a drain region;

wherein a top portion of the source structure and a top portion of the drain structure are within and abut the body thickness.

[c9] The transistor of claim 8, wherein the first layer of the buried insulator is at least as thick as the semiconductor layer.

[c10] The transistor of claim 8, wherein the semiconductor layer comprises single crystal silicon.

[c11] The transistor of claim 8, wherein the buried insulator comprises three layers, wherein a second layer is different from the first layer and a third layer.

[c12] The transistor of claim 11, wherein the first layer comprises silicon dioxide, wherein the second layer comprises silicon nitride, wherein the third layer comprises silicon dioxide.

[c13] The transistor of claim 8, wherein the first recess and the second recess stop on a

second layer of the buried insulator.

[c14] The transistor of claim 8, wherein the body comprises a fin structure that comprises a top fin structure surface and a bottom fin structure surface that define a fin structure thickness, wherein the top portion of the source structure and the top portion of the drain structure are within and abut the fin structure thickness.

[c15] A semiconductor wafer comprising a silicon layer on a buried insulator that comprises a first buried insulator layer on a second buried insulator layer different from the first buried insulator layer, wherein the first buried insulator layer is at least as thick as the silicon layer.

[c16] The semiconductor wafer of claim 15, wherein the first buried insulator layer comprises silicon dioxide.

[c17] The semiconductor wafer of claim 15, wherein the second buried insulator layer comprises silicon nitride.

[c18] The semiconductor wafer of claim 15, further comprising a transistor.

[c19] The semiconductor wafer of claim 18, wherein the transistor comprises a source structure and a drain structure recessed through the first buried insulator layer.

[c20] The semiconductor wafer of claim 18, wherein the transistor further comprises a fin structure.